DRONACHARYA
College of Engineering

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department:ECE

Academic Session: 2017-18 (Jan-June 2018)

Lesson Plan for the Semester started w.e.f 08.01.2018

Subject with code:VLSI DESIGN(EE-306-F)

Name of Faculty with designation :Krishanu Kundu,Asst.Prof

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Academic activity	Test / assignment
January	10.01.2018 Wednesday	VI-ECE/EEE	1	Introduction to MOSFETs -Description of MOSFETs -Operation of Enhancement mode & Depletion mode MOSFET -Description & structure of n-MOS & p-MOS -Description & structure of CMOS	……	Assignment of 02 Ques. given
January	11.01.2018 Thursday	VI-ECE/EEE	1	Equivalent circuit of n-MOS ,p-MOS &CMOS -Threshold voltages for n-MOS and p-MOS Drain current characteristics of E-type & D-type n-MOSFET -Identification of regions of operation of the MOSFETs -Conductance characteristics of E-type & D-type n-MOSFET	……	Assignment of 02 Ques. given
January	17.01.2018 Wednesday	VI-ECE/EEE	1	structure of Enhancement mode n-MOSFET -Polarities of voltages applied to Gate, Drain, Source & Substrate. Formation of channel in enhancement mode MOSFET Derivation of mathematical expression for Drain current IDS for n-MOS and p-MOS	……	Assignment of 02 Ques. given
January	18.01.2018 Thursday	VI-ECE/EEE	1	Diagram of structure of n-MOS & p-MOS & voltage polarities. Definition of Threshold voltage & substrate bias.Work function difference between gate and Si Fermi level potential between inverted surface and bulk Si Expression for Threshold voltage Meaning & Expression of Body effect	……	Assignment of 02 Ques. given
January	24.01.2018 Wednesday	VI-ECE/EEE	1	Subthrehold region -Channel length Modulation -Mobility variation -Fowler-Nordheim Tunnelling -Drain Punchthrough -Impact ionization-Hot electrons	……	Assignment of 02 Ques. given

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January	25.01.2018 Thursday	VI-ECE/EEE	1	MOS device transconductance - figure of merit - Small signal equivalent model AC characteristics - Output conductance - Channel resistance	……	Assignment of 02 Ques. given
January	23.01.2018 Tuesday	VI-ECE/EEE	1	Different configurations of MOS switches and MOS loads -Output characteristics for different ratios of (W/L)driver/ (W/L)	……	Assignment of 02 Ques. given
January	1.02.2018 Thursday	VI-ECE/EEE	1	Principle & Working of Latch –up circuit Latch-up circuit Model V-I characteristics of TTL BiCMOS inverter Circuit	……	Test
January	7.02.2018 Wednesday	VI-ECE/EEE	2	Derivation of n-MOS inverter transfer characteristic & threshold voltage of inverter. -Effect of variation of (Z pu / Zpd) on the transfer characteristic	……	Assignment of 02 Ques. given
January	8.02.2018 Thursday	VI-ECE/EEE	2	Basic principle of CMOS Working of CMOS DC characteristics of CMOS βn / βp ratio Noise Margin CMOS Inverter as an Amplifier	……	Assignment of 02 Ques. given
February	21.02.2018 Wednesday	VI-ECE/EEE	2	Basic configuration of MOS switch with load resistance RL -Configuration of MOS switch and n-MOS depletion mode transistor pull up -Configuration of MOS switch and n-MOS enhancement mode transistor pull up	……	Assignment of 02 Ques. given
February	22.02.2018 Thursday	VI-ECE/EEE	2	MOS AS PASS TRANSISTOR & DETERMINATION OF PULL UP/PULL DOWN RATIO FOR n-MOS INVERTER DRIVEN BY ANIOTHER n-MOS INVERTER /PASS TRANSISTOR	……	Assignment of 02 Ques. given
February	28.02.2018 Wednesday	VI-ECE/EEE	2	A generic static load inverter -The Pseudo –n MOS inverters -Saturated load inverters using n MOS transistor load -The Cascode inverter -TTL interface inverter	……	Assignment of 02 Ques. given

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March	**7.03.2018 Wednesday**	**VI-ECE/EEE**	2	**A simple inverter (basic gates) transistor model -The rule for designing STICK DIAGRAM for pMOS and nMOS transistors -Substitution of stick bar in place of transistors**	……	**Assignment of 02 Ques. given**
March	**8.03.2018 Thursday**	**VI-ECE/EEE**	2	**Discussion on Lambda based rules An inverter layout -The distance gap within different construction material used for transistor model. -Design Rule Check -Channel length parameter -Latest technology trends**	……	**Assignment of 02 Ques. given**
March	**14.03.2018 Wednesday**	**VI-ECE/EEE**	2	**Super Buffers classification,BiCMOS Features - Gates design BiCMOS -Steering Logic through multiplexer -Few examples implementation by Steering logic**	……	**Test**
March	**15.03.2018 Thursday**	**VI-ECE/EEE**	**3**	**Combinational circuit Boolean expression minimization - Expression realization with the pMOS - Expression realization with the nMOS - Realization of digital circuits using cMOS Tristate Inverter**	……	**Assignment of 02 Ques. given**
March	**28.03.2018 Wednesday**	**VI-ECE/EEE**	**3**	**V-I CMOS Logic StructuresClocking Strategies Estimation of R, Resistance of Nonrectangular Regions Contact and Via Resistance Refresh loop ,Parallel load mode, Shift right mode Shift left mode,Parallel out put,Isolation of inverters**	……	**Assignment of 02 Ques. given**
March	**4.04.2018 Wednesday**	**VI-ECE/EEE**	**3**	**Analytic Delay Models of -Rise Time, tr, -Fall Time, tf, -Delay Time, td Empirical Delay Models**	……	**Test**
April	**5.04.2018 Thursday**	**VI-ECE/EEE**	**4**	**Introduction to CAD tools,Use of CAD tools Introduction to VHDL:Structural Modeling Data Flow Modeling ,Behavioral Modeling OBJECTS,CLASSES,DATA TYPES, OPERATORS**	……	**Assignment of 02 Ques. given**
April	**11.04.2018 Wednesday**	**VI-ECE/EEE**	**4**	**Libraries and Packages ,Overloading Programmable Logic Devices. • Programmable Array Logic • Programmable Logic Array • FPGA • ROM**	……	**Assignment of 02 Ques. given**

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April	12.04.2018 Thursday	VI-ECE/EEE	4	ROM(Read Only Memory) as PLD PLA(Programmable Logic Array) and PAL(Programmable Array Logic) FPGA(Field Programmable Gate Array) CPLD's(Complex Programmable Logic Devices)	……	Test